Sheet 1 of 1

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT			ATTY DOCKET NO. SERIAL NO.							
			536.009.23	U.S. SERIAL NO. 10/542,938						
			APPLICANT: Eckhard Grass et al.							
			FILING DATE:	ART UNIT:						
			July 20, 2005	To Be Assigned						
	·	UNITED STA	TES PATENT DOCUMENT	s						
EXAM. INITIAL	DOCUMENT NUMBER	DATE	INVENTOR/ASSIGNEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE				
		<u></u>		·						
		FOREIGN	PATENT DOCUMENTS							
					SUBCLASS	TRANSLATION YES/NO				
	OTHER DOCUMEN	TS (INCLUDING	AUTHOR, TITLE, DATE, P	ERTINENT	PAGES, ETC.)					
/JB/	IEEE Std. 802.11a-1999 (supplement to IEEE Std 802.11-1999); PART 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specification; High-speed Physical Layer in the 5 GHz Band.									
/JB/	2002 IEEE; Simon Moore et al., Computer Laboratory, Univ. of Cambridge, UK, Simon.Moore@cl.cam.ac.uk; <i>Point to Point GALS Interconnect</i>									
/JB/	Ran Ginosar et al, VLSI Systems Research Center, Technion - Israel Inst. of Technology, Haifa 32000, Israel; Adaptive Synchronization.									
/JB/		The Association for Computing Machinery, 1515 Broadway, New York, NY 10036; Proceedings of the 38th Design Automation Conference.								
/JB/		Eckhard Grass et al, University of Oulu; IEEE Personal Communications, December 2001, On the Single-Chip Implementation of a Hiperlan/2 and IEEE 802.11 a Capable Modem.								
/JB/	Daniel M. Chapiro, Department of Computer Science, Stanford Univ., Stanford, CA 94305, October 1984, UB/TIP Hannover, Report No. STAN-CS-84-1026; Globally-Asynchronous Locally-Synchronous Systems.									
Examiner (To	o be assigned) /Ji Bae,	/ (08/11/2007)	Date:							

n

Sheet 1 of //

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT				ATTY DOCKET NO. 536.009.23	SERIAL NO. (PCT/EP03/14959) To be assigned 10/542938							
			APPLICANT: Eckhard Grass et al.									
			FILING DATE:	ART UNIT: To Be Assigned								
								December 29, 2003				
UNITED STATES PATENT DOCUMENTS												
EXAM. INITIAL		DOCUMENT NUMBER	DATE	INVENTOR/ASSIGNEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE					
		·										
		·										
			FOREIGI	N PATENT DOCUMENTS								
						SUBCLASS	TRANSLATION YES/NO					
							-					
		OTHER DOCUMEN	TS (INCLUDING	AUTHOR, TITLE, DATE, PE	ERTINENT	PAGES, ETC.)						
/JB/	1	Tormod Njolstad et al., IEEE 2001, A SOCKET INTERFACE FOR GALS USING LOCALLY DYNAMIC VOLTAGE SCALING FOR RATE-ADAPTIVE ENERGY SAVING, Norwegian Univ. of Science and Technology (NTNU), Norway.										
/JB/		Schengxian Zhuang et al., IEEE 2002, Asynchronous Data Communication with Low Power for GALS Systems, Electronics Systems, Dept. of Electrical Engineering, Linkoping, Sweden.										
/JB/		Jens Muttersbach, Globally-Asynchronous Locally-Synchronous Architecture for VLSI Systems, (A dissertation submitted to the Swiss Federal Institute of Technology, Zurich, Diss. ETH No. 14155).										
/JB/		Kenneth Y. Yun, <i>Pausible Clocking: A First Step Toward Heterogeneous Systems,</i> Dept. of Electrical and Computer Engineering University of California, San Diego.										
/JB/		S.W. Moore et al., IEEE 2000, Self Calibrating Clocks for Globally Asynchronous Locally Synchronous Systems, University of Cambridge, Cambridge, United Kingdom.										
/JB/	2	Jens Muttersbach et al., IEEE 2000, <i>Practical Design of Globally-Asynchronous Locally-Synchronous Systems</i> , Integrated Systems Laboratory, Swiss Federal Institute of Technology Zurich, Switzerland.										
/JB/	3	David S. Bormann, et al., IEEE 1997, Asynchronous Wrapper for Heterogeneous Systems, Department of Electricial and Electronics Engineering Imperial College of Science, Technology and Medicine, United Kingdom.										
Examiner (To b	e assigned) /Ji Ba	ie/ (08/11/2007)	Date:			:					